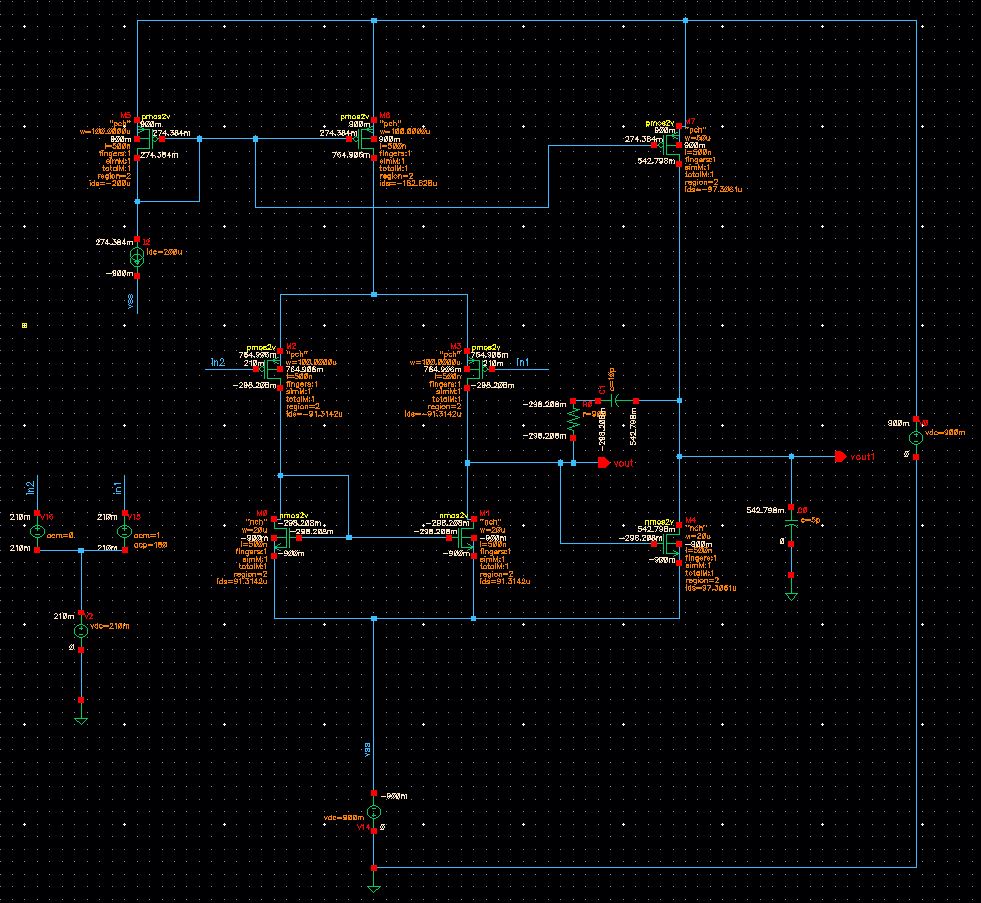
***PROJECT AIM (SUNNY) -***

***SCHEMATICS WITH EXPLANATION (HERAMB) -***



We are using the above schematics for our project which is two stage opamp with a differential input and single ended output. We are using current mirror circuit for biasing. We are using an ideal current source in current mirror which is of 200uA. For our schematics vdd is +0.9V and Vss  is -0.9V as required for project. We are also using the miller compensation between two stages for pole splitting.

Following are the expressions used for calculating gain.

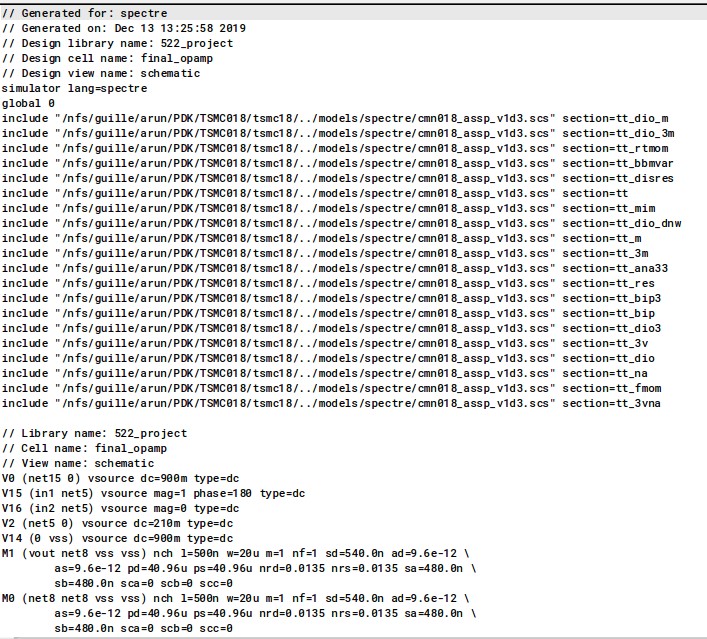
Gain = gm2\*(rds3||rds1) \* gm4\*(rds4||rds7)

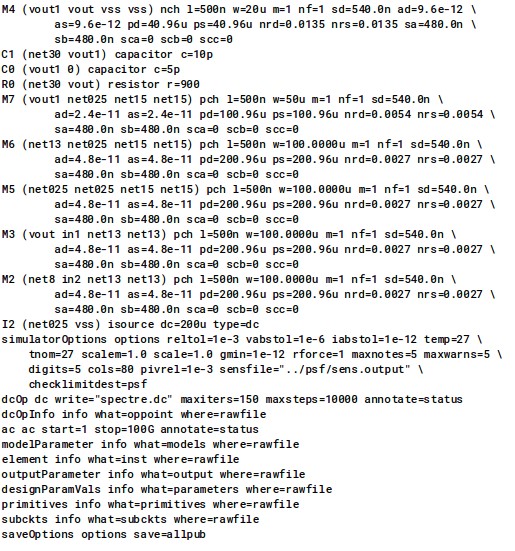
 gm2\*(rds3||rds1) is the gain of first stage and gm4\*(rds4||rds7) is the gain of second stage. As we can see that gain depends mainly on two things, one is gm of input transistor and rds of output transistors. So we kept the width of input transistors high to get high gm and then we increased length of transistors to 500nm to increase the rds of transistors which helped us to achieve the required gain. We are using compensation capacitor of 10pF and resistor of 900 ohms.

***SIZES OF ALL THE TRANSISTORS (HERAMB) -***

|  |  |  |
| --- | --- | --- |
| **MOSFETS** | **WIDTH (W)** | **LENGTH (L)** |
|  |  |  |
| **M0** | **20u** | **500n** |
| **M1** | **20u** | **500n** |
| **M2** | **100u** | **500n** |
| **M3** | **100u** | **500n** |
| **M4** | **20u** | **500n** |
| **M5** | **100u** | **500n** |
| **M6** | **100u** | **500n** |
| **M7** | **50u** | **500n** |

***NETLIST (HERAMB) -***

******

******

***OUTPUTS (SUNNY) -***

***Madarchod***

***bhak lavdya***

***RESULTS (SUNNY) -***

Gain (Calculated) = 73.03 dB

Gain (Simulated) = 73.14 dB

Vcm max = 210mv

Vcm min = -700m